Operation Manual

X.50 FRAME

Annex to TSW200E1's Operation Manual

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Summary

1 - Introduction

X.50 is a frame structure used at 64 Kbps to allow the transportation of many data channels with smaller rates within the 64 kbps synchronous bandwidth. The X.50 structure has two divisions: 2 and 3. The division 2 X.50 frame is composed of 80 octets and defines five different speeds. The division 3 X.50 frame is composed of 20 octets, as defined in Appendix A, and it defines four different speeds and many transmission combinations.

In the X.50 operation mode, the TSW200E1 allows circuit, structure and error analysis of the data transmitted by a 64 Kbps X.50 channel, divisions 2 and 3.

For all tests, the counter options are: BIT ERROR, FAS ERROR, SLIP (following ITU-T Rec. G.822), RX RATE, TIME, SIGNAL LOSS, AIS, FAS LOSS, NO CLOCK, PAT LOSS and REMOTE ALARM.

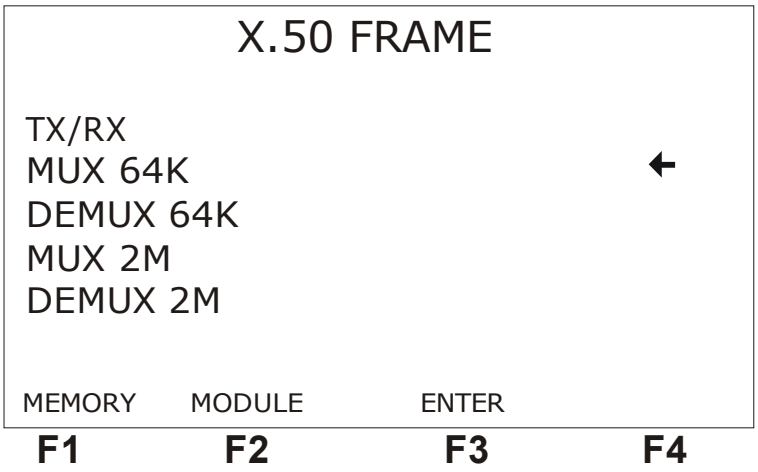
For the BIT ERROR and FAS ERROR counters, there is also an error analysis known as errored seconds counting (ERRORED SEC.), severely errored seconds counting (SEV.ERR.SEC.), degraded minutes (DEGRADED MIN.), available seconds (AVAILAB.SEC.), unavailable seconds (UNAVAIL.SEC.), error-free seconds (ERR. FREE SEC.) and the rate between the errored bits number and the total number of transmitted bits (BER) according to ITU-T Rec. G.821.

Some of the characteristics of this module are:

- Interfaces: V.24/RS232, V.35/V.11, V.36/V.11, X.21/V.11, RS530, G.703 Codirectional and 2Mbps G.703;
- Generated sequences: 63 (2^6-1), 511 (2^{9-}1), 2047 (2^{11}-1), 2^{15}-1, 2^{20}-1, Mark, Space, ALT M/S and USER, in the NORMAL and INVERTED modes;
- Independent selection of transmission and reception octets;
- Programmable idle code;
- The BERT/IDLE status bits are programmable.

2 - X.50 Module Operation

When choosing the X.50 Module on the TSW200E1 Module Screen, the following screen will be shown. At this screen, it is possible to choose which kind of X.50 test will be carried out and if it will be run at 64Kbps or inside the PCM frame structure at 2Mbps. The choice is made by moving the cursor to the desired position and by pressing the <F3> (ENTER) key.

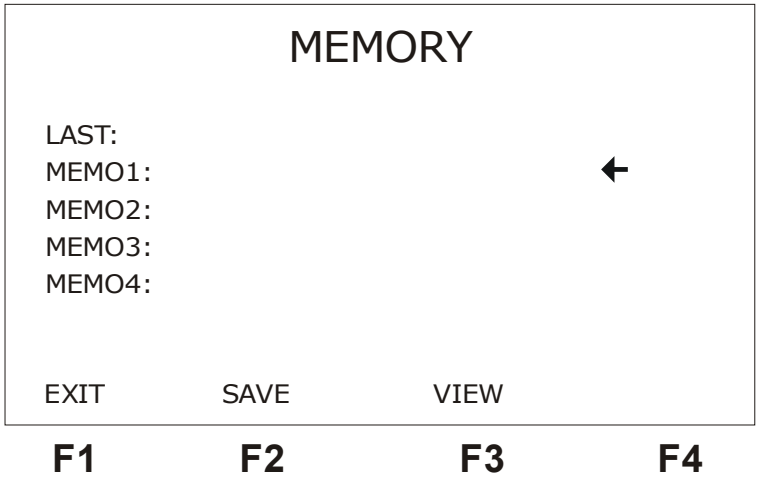


It is possible to carry out five tests: TX/RX, MUX 64K, DEMUX 64K, MUX 2M and DEMUX 2M.

The detected errors and alarms are counted and indicated. These counters are displayed on the screen and the occurrence of an error or alarm is indicated using leds. It is important to know that some errors and alarms are the same in the X.50 and PCM frames, and both are indicated using leds, but only those related to X.50 frames are counted in this module.

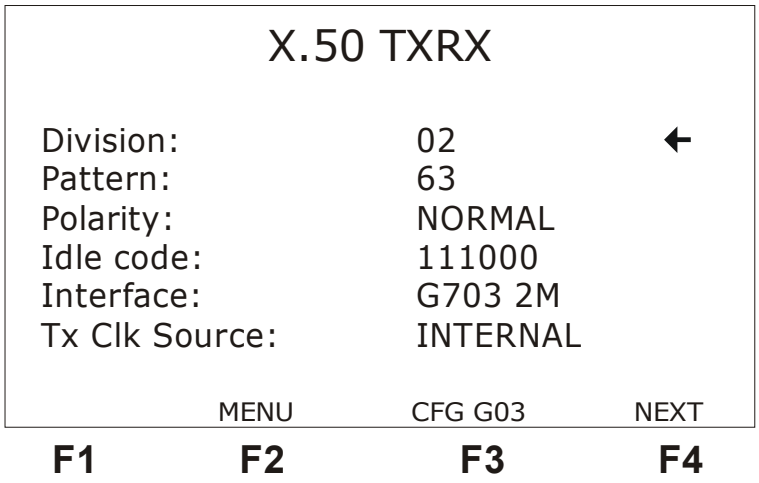
The following sections describe the equipment configuration procedures, the configuration parameters and the running of the TX/RX, MUX and DEMUX tests for the speeds of 64Kbps and 2Mbps.

The X.50 module has memory to store up to four tests. The memory is accessible from the previous screen and by using the <F1> (MEMORY) key. The error and alarm counters and the G.821 Recommendation analyses can be stored in memory. The last test to be run is always stored in the LAST memory position and it is possible to store it in four different memory positions (MEMO1 to 4). To do this use the <F2> (SAVE) key. To visualise the contents of a memory position, use the <F3> (VIEW) key. The navigation on the memory screens is done in a similar way as for the running test, which is described at the subsequent sections.



2.1 - TX/RX X.50 Test Configuration

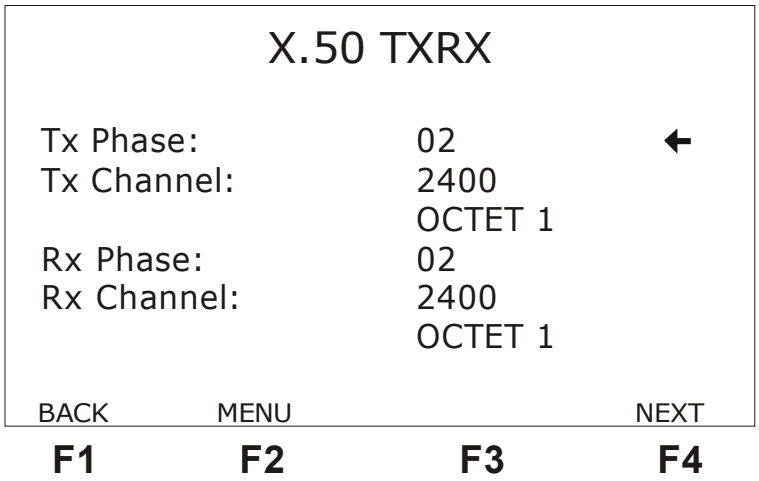
Before starting the TX/RX X.50 test, it is needed to correctly configure the test set. This configuration is done by choosing many parameters, as shown on the screens below. Use the <F1> (BACK) or <F4> (NEXT) keys to alternate among these screens. The parameters shown on these screens will be described next. To change the options move the cursor to the appropriate line and use the ← and → keys or the DATA key to perform editing.



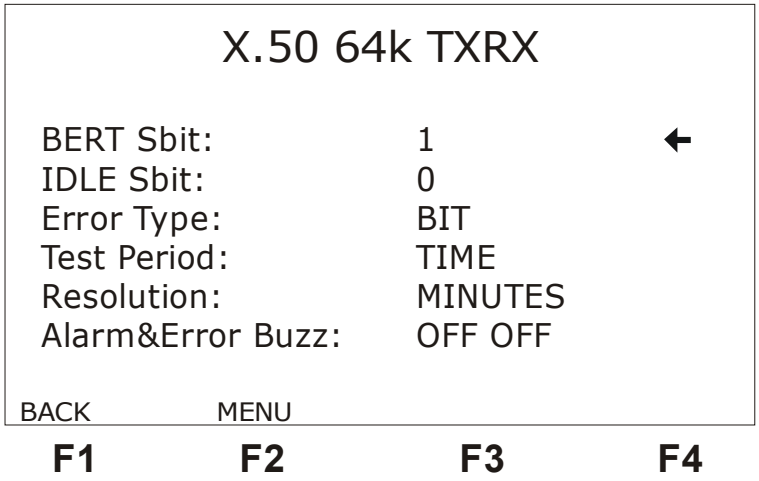
- Division: Selects the kind of X.50 to be used. It is possible to choose division 02 or 03.
- Pattern: Selects the pattern to be transmitted in the selected channel. The chosen pattern can be pseudo-random, with length of 63, 511, 2047, 215-1, 220-1 bits, or fixed as Mark, Space or alternating Mark (M) / Space (S). The user can also opt for the USER pattern, where he or she can generate any test sequence with up to 16 bits in length. Editing of the USER pattern is done as for the BERT/BLERT mode.
- Polarity: Selects the polarity of the transmitted signal as NORMAL, where the bits of the standard sequence selected are normally transmitted or INVERTED, where the bits are all inverted.
- Idle Code: Selects the idle code to be transmitted in the non-selected channels. Press

the DATA key to edit. The keys ← and → move the cursor to the bit that must be changed. To exit the editing mode, press <F4> (ENTER) to confirm editing or <F1> (EXIT) to cancel editing.

- Interface: This option selects the interface through which the test pattern will be sent. The options are V.24/RS232, V35, V36, X.21, RS530, G.703 Codirectional and G.703. 2M. When choosing the G.703-2M interface, it is necessary to configure many parameters. To do this, press <F3> (CFG G703). For the detailed description of these parameters, please see the following pages of this manual.
- Tx Clock Source: Selects the origin of the transmission clock. For external clock, the transmission data are synchronized to the clock provided by the external circuit, which must be configured for internal or regenerated clock. For internal clock, the Test Set itself provides the transmission clock. In this case, the external circuit must be prepared to accept external clock.

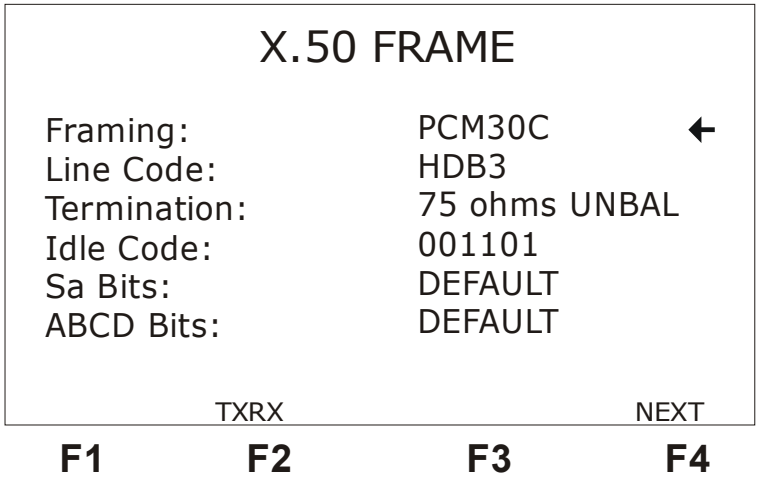


- Tx Phase: Selects the number of the transmission phase, from 01 to 05.
- Tx Channel: Selects the channel or octet and the transmission rates. See Appendix A for the possible combinations.
- Rx Phase: Selects the number of the reception phase, from 01 to 05.
- Rx Channel: Selects the channel or octet and the reception rates. See Appendix A for the possible combinations.

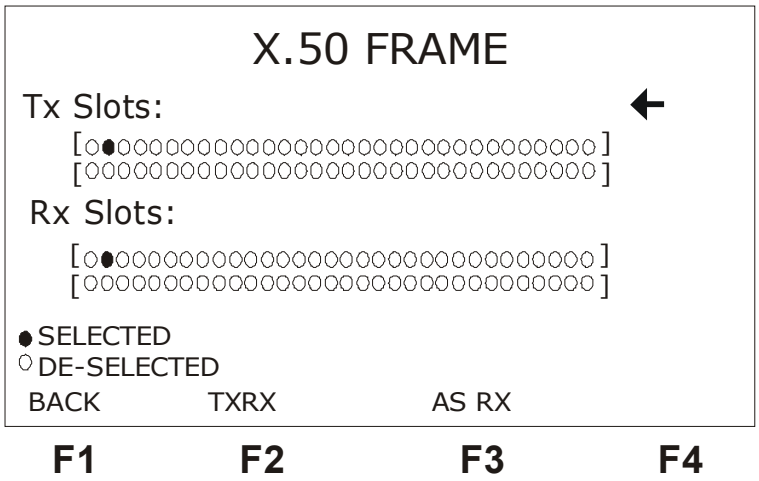


- BERT Sbit: This option allows choosing the state in which the status bit must be in the octet that transmits data. The options are 0 and 1.
- IDLE Sbit: Allows choosing the state in which the status bit must be in the octets that transmit idle code. The options are 0 and 1.
- Error Type: Allows choosing the kind of error that will be inserted on the test when the error key is pressed. The available options are: BIT, FAS and ALARM.
- Test Period: Defines the test duration. The selectable options are CONTINUOUS, for a continuous test during an undetermined amount of time, or TIME, for a test limited in time by a programmable timer. To choose the duration of the test, select the TIME option and press the DATA key. Use the alphanumeric keys and the arrow keys to edit. To exit the editing mode, press <F4> (ENTER) to confirm editing or <F1> (EXIT) to cancel editing.
- Resolution: Allows choosing the histogram resolution, which can be in MINUTES or HOURS.
- Alarm & Error Buzz: Allows the user to activate or not the buzzers indicating error or alarm. The choice must be made as OFF OFF, ON OFF, OFF ON or ON ON. When ON, the buzzer is active; and when OFF, the buzzer is inactive.

When the <F3> label displays the option CFG G703, if it is pressed, the following screens are shown.



- Framing: Selects the frame structure. The structures are PCM30, PCM30C, PCM31 and PCM31C.
- Line Code: Allows the user to choose the line code as HDB3 or AMI.
- Termination: The cable termination impedance can be chosen as 75 ohms UNBAL, 120 ohms BAL, HIGH-Z UNBAL or HIGH-Z BAL.
- Idle Code: Selects the Idle Code to be transmitted in the deselected channels. Press the DATA key to edit.
- Sa Bits: The DEFAULT option keeps all bits at 1. The USER option allows programming the NFAS (Sa) word.
- ABCD Bits: The DEFAULT option keeps all the ABCD bits at 1000. The USER option allows programming the 30 ABCD words of timeslot 16, but only for the PCM30 and PCM30C structures.



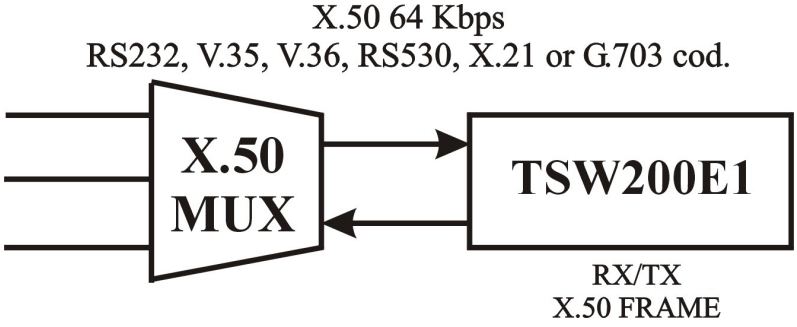
- Tx Slots: Selects the timeslot(s) for transmission, from 01 to 31.
- Rx Slots: Selects the timeslot(s) for reception, from 01 to 31.

To return to the selected test configuration screen, press the <F2> key.

2.2 - Performing the X.50 TX/RX Test at 64kbps

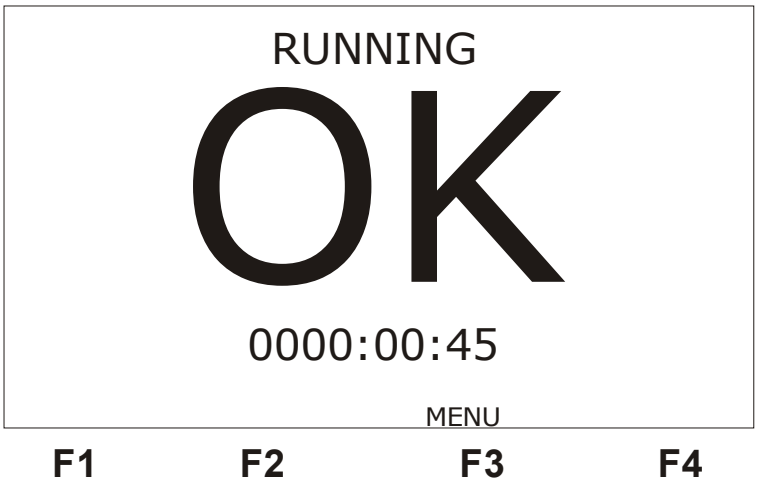
The objective of the TX/RX test is to do the circuit analysis, data structure analysis and check error occurrence in the data transmitted by an X.50 channel. To do that, all channels are observed, checking the frame alignment signal (FAS) word and if there are errors in the transmitted data.

The figure below exemplifies a way of performing the X.50 test.



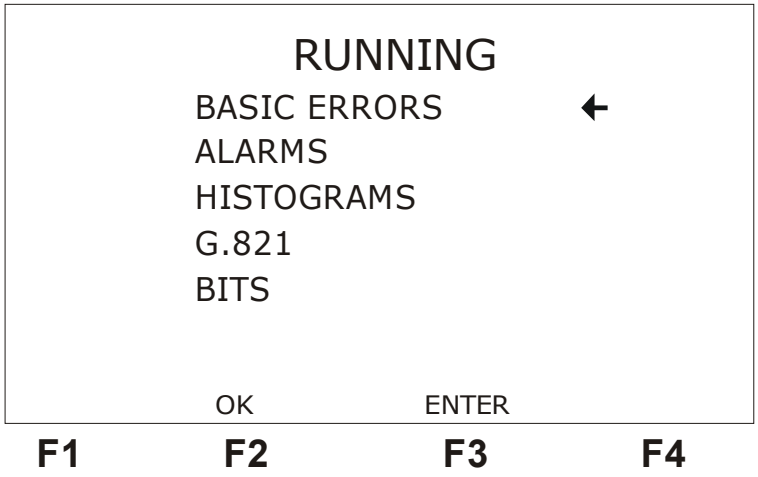
The test is started by pressing the START/STOP key from any of the screens shown on section 2.1. To end the test, press the same key from any of the screens of the test in progress.

The OK screen, shown below, is exhibited when the test is started. The equipment displays this screen until an error or alarm is detected or until the user intervenes.



When detecting an error or alarm, the test set automatically changes the screens, displaying the error or alarm counter. From the moment the error or alarm is detected, the OK screen is not accessible anymore.

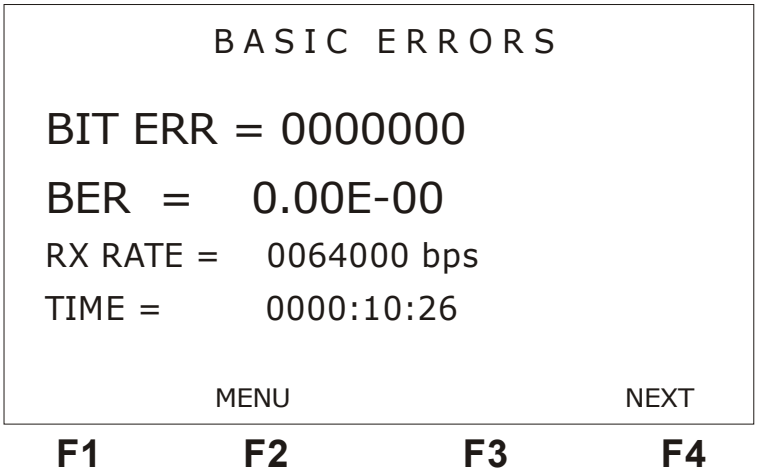
From the OK screen it is possible to check the error screens, alarms or bits by pressing the <F3> key and thus changing to the following menu screen.



From this screen, it is possible to access the error, alarm, histograms, G821 analysis or bit screens. To do this, move the cursor to the appropriate line and press <F3> (ENTER).

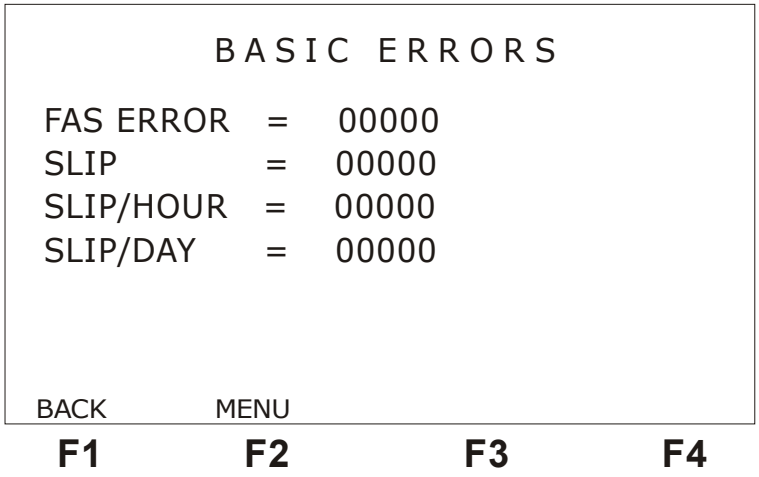
When choosing the BASIC ERRORS option, the first error screen is as shown in the figure below. This screen presents the following counters:

- BIT ERR: Counts the total number of errored bits in the received data.
- BER: Shows the rate between errored bits and received bits.
- RX RATE: Displays the data receive rate.
- TIME: Displays the elapsed test time.



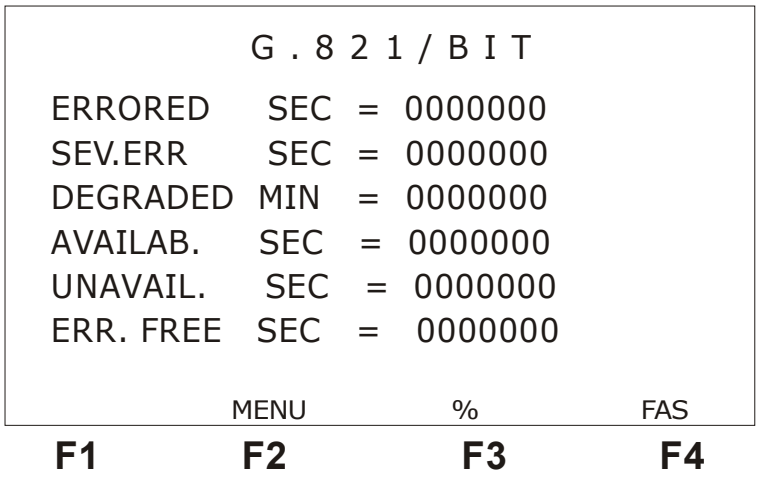
From this screen, it is also possible to press <F4> (NEXT) to go to the second error screen. Press <F3>(MENU) to go back to the menu screen.

The second error screen is shown below. It presents the following error counters:



- FAS ERR: indicates the total number of FAS errors that occurred in the test in progress.
- SLIP: indicates clock slippage, that is, a misalignment between the receive and transmit clocks. Valid only for pseudo-aleatory sequences.
- SLIP/HOUR: indicates the rate between SLIPS to hours (G.822).
- SLIP/DAY: indicates the rate between SLIPS to days (G.822).

When choosing the ITU-T Rec. G.821 error analysis screen, the screen is as shown at the figure below. The TSW200E1 evaluates the ITU-T Rec. G 821 parameters for the BIT ERROR and FAS ERROR counters. There are screens like this one for BIT and FAS errors. The G.821 counter screen is presented on the figure below. The first one displayed refers to the bit errors. Press <F4> (FAS) to go to the FAS error screen.



The G.821 counters are the following:

- ERRORED SEC: displays how many 1-second intervals have at least an error.
- SEV. ERR. SEC: displays how many 1-second intervals have the bit error rate greater than 1.10^{-3}.
- DEGRADED MIN: displays how many 1-minute intervals have error rates greater

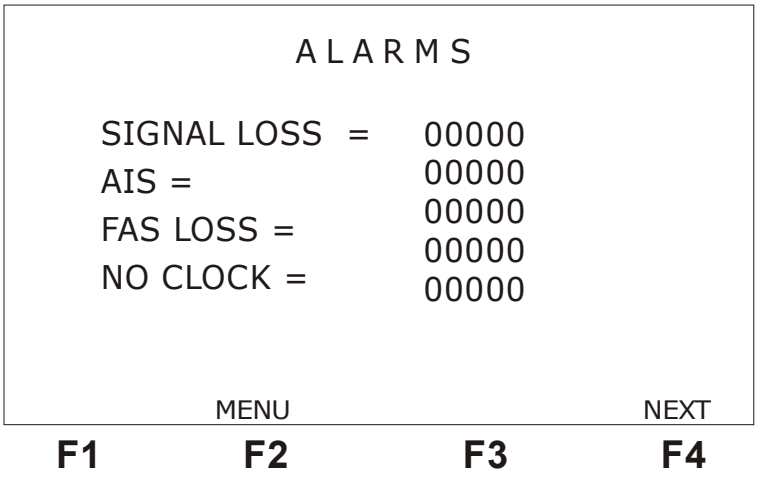
than 1.10^{-6}.

- AVAILAB.SEC: number of available test seconds.
- UNAVAIL.SEC: displays the number of unavailable seconds during the test.
- ERR.FREE SEC: displays how many 1-second intervals were error-free.

Press <F2> (MENU) to go back to the menu screen. To visualise these counters in percent values, press <F3> (%). The description of each value displayed in the screen of percent values follows.

- ERRORED SEC: indicates the rate between the number of 1-second time intervals that have at least one error and the available measuring time (according to Rec. G.821).
- SEV. ERR. SEC: indicates the rate between the number of 1-second time intervals where the bit error rate is greater than 1.10^{-3} and the available measuring time (according to Rec. G.821).
- DEGRADED MIN: indicates the rate between the number of 1-minute time intervals where the error rate is greater than 1.10^{-6} and the available measuring time (according to Rec. G.821).
- AVAILAB. SEC: indicates the rate between the available measurement seconds and the total elapsed time. The available measurement seconds are given by the difference between the total measurement elapsed time and the unavailable time.
- UNAVAIL. SEC: indicates the rate between the unavailable measurements seconds and the total elapsed time. The unavailable time is defined as the time when the bit error rate is greater than 1.10-3, during one-second intervals, for 10 consecutive seconds (ITU-T Recommendation G.821).
- ERR. FREE SEC: indicates the rate between the number of error-free 1-second time intervals and the available measurement time.

When selecting the ALARMS option in the Menu screen, the following screen is presented:



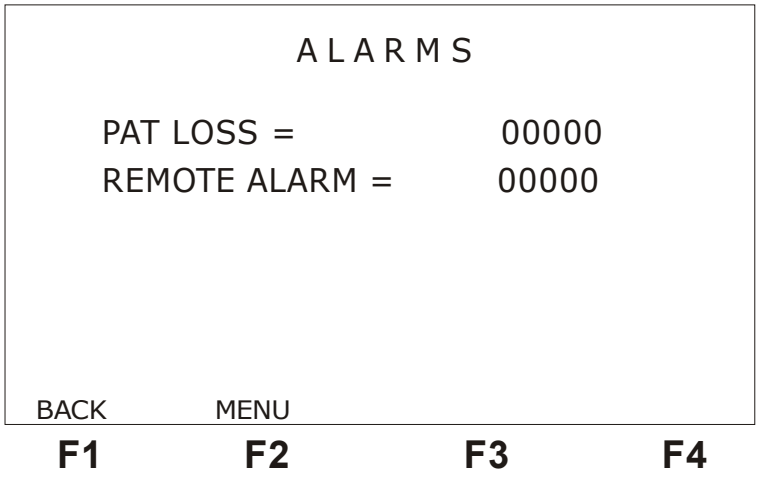
It displays the following counters.

- SIGNAL LOSS: indicates the total number of times that the 64 kbps stream was absent during the test in progress.

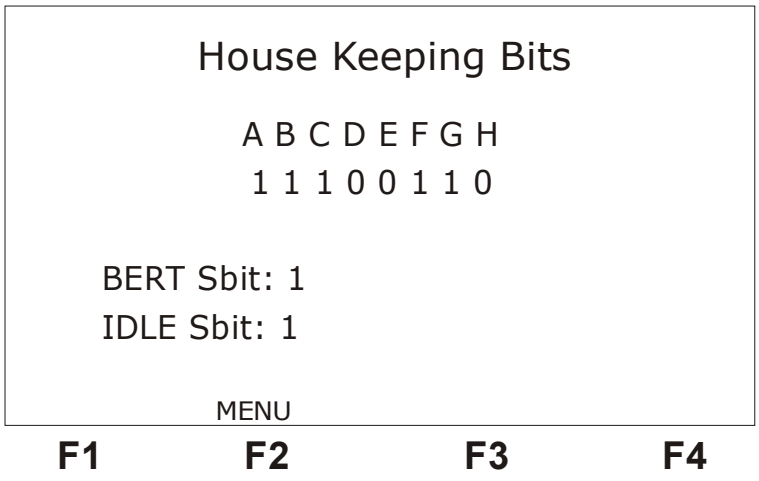
- AIS: indicates the total number of times that the alarm indication signal occurred during the test in progress.
- FAS LOSS: indicates the total number of frame sync losses accounted for during the test in progress.
- NO CLOCK: indicates absence of the receive clock.

From this screen, it is possible to reach the second alarms screen by pressing <F4> (NEXT). The second screen is presented in the following figure. The displayed counters are:

- PAT LOSS: Indicates the number of pattern sync losses. That means that the expected sequence is not arriving.
- REMOTE ALARM: Indicates the number of times that the remote alarm was sent (bit A is reset, indicating remote alarm).



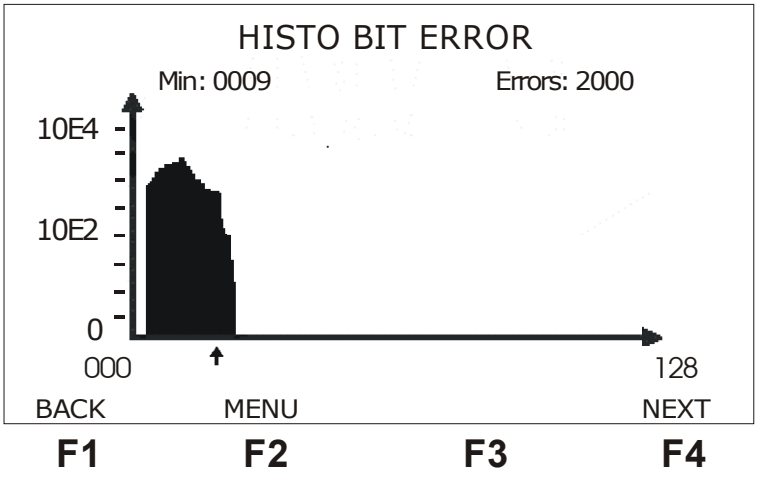
Selecting the BITS option in the menu screen displays the following screen.



This screen allows visualisation of the maintenance bits (A, B, C, D, AND, F, G and H), which are being received and the BERT/IDLE Sbits status. If division 3 is chosen, only the A and BERT/IDLE Sbits bits are displayed. Press <F3>(MENU) to go back to the OK screen or to the MENU screen.

Selecting the HISTOGRAMS option at the MENU screen displays the histograms for each

alarm and error occurrence. The histograms are graphical displays of the number of errors or alarms versus time. For each type of error or alarm that can occur for a certain configuration, a histogram is presented. Each histogram column displays the number of errors or alarms that occurred in that minute, or hour, according to the resolution chosen at the configurator.



There is a small cursor below the graphic that points to the column. In the upper part of the display, right below the title, there is the minute or hour corresponding to the column pointed to by the cursor and the number of errors or alarms that occurred in that minute (according to the plotted graphic). To scroll the cursor over the graphic, use the ← and →keys to move the cursor on a column basis or the ↑ and ↓ keys to move the cursor 16 positions at a time.

From the histogram screen it is possible to access the next histogram screen by pressing <F4>(NEXT). To go back to the previous screen, press <F1> (BACK). Or else, to go back to the Menu screen, use the <F3> (MENU) key.

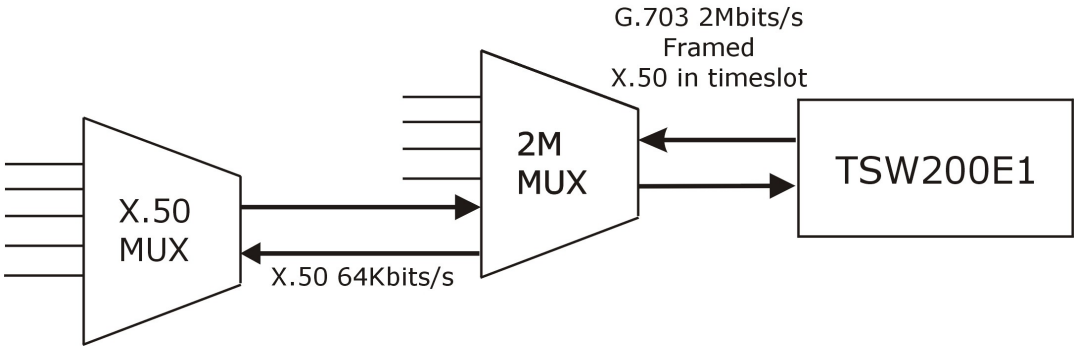
According to the type of error or alarm chosen and to the selected resolution, the histogram scale can be linear or logarithmic. The maximum number of errors or alarms that can be displayed in a histogram is 65534, but most counters can count more than that.

The histogram is limited to 3663 positions. That means that a histogram can monitor a test of up to 61 hours. But the maximum number of errored minutes that can be displayed within the 61 test hours is 70.

2.3 - Perfoming the X.50 TX/RX Test at 2Mbps

When the G.703 interface is selected, the TX/RX test consists in the analysis of the circuit, data structure and data error of an X.50 frame structured channel allocated within a 2 Mbps PCM frame slot. To achieve this purpose, every channel is observed, checking the frame sync word (FAS) and if there is any error in the transmitted data.

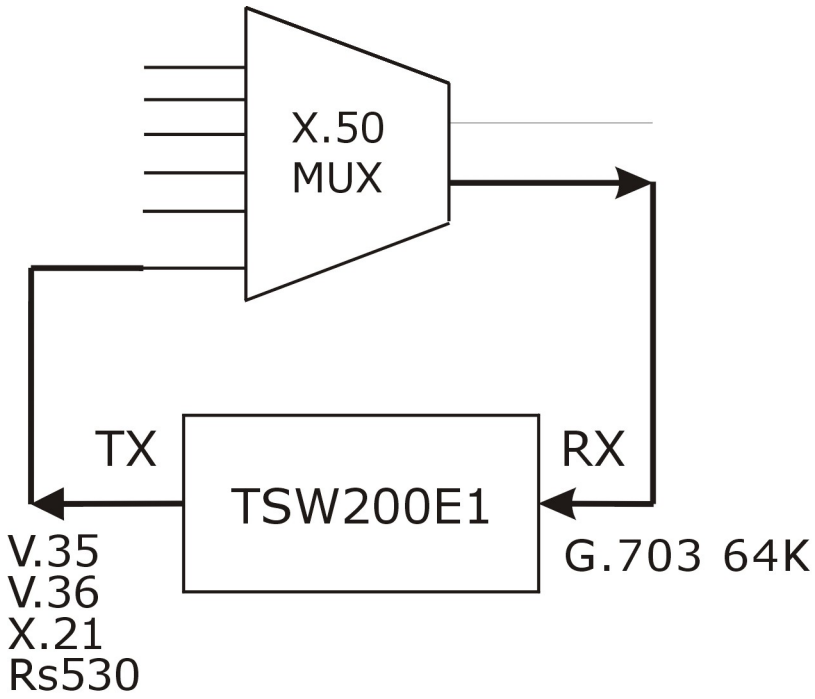
The following figure exemplifies how to run the TX/RX X.50 test at 2Mbps.



The results are displayed in the same way as described in Section 2.2.

2.4 - Configuring and Running the X.50 MUX Test at 64kbps

The figure below exemplifies running the MUX test at 64kbps.



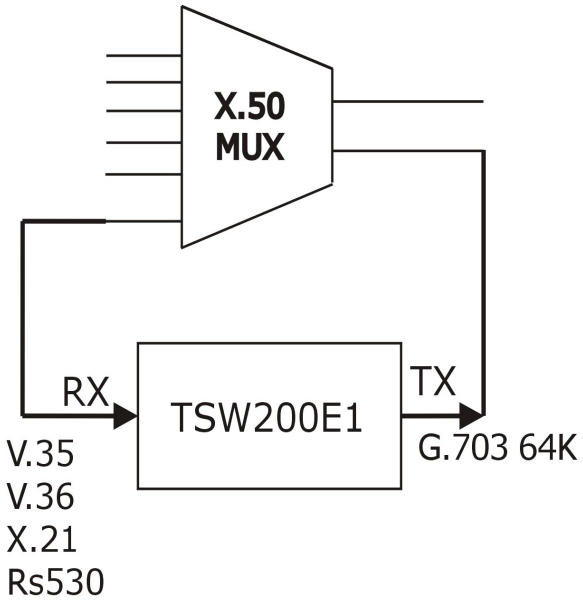
The test consists in sending a data pattern and checking if this same pattern is received in the X.50 frame structure. The test pattern is sent to the multiplexer via the interface that can be user-chosen as V.35/V.11, V.36/V.11, X.21/V.11 or RS530. The reception of the X.50 data stream is always through the G.703 64kbps (Codirecional) interface.

Configuring the MUX test is very similar to configuring the TX/RX test, but only the transmission interface and reception-related parameters are changed. The clock source is always external, for it must be provided by the X.50 Mux.

The test results are presented in the same way as for the TX/RX test. Please check the previous section for more details.

2.5 - Configuring and running the X.50 DEMUX Test at 64kbps

The figure below exemplifies running the DEMUX test at 64kbps.



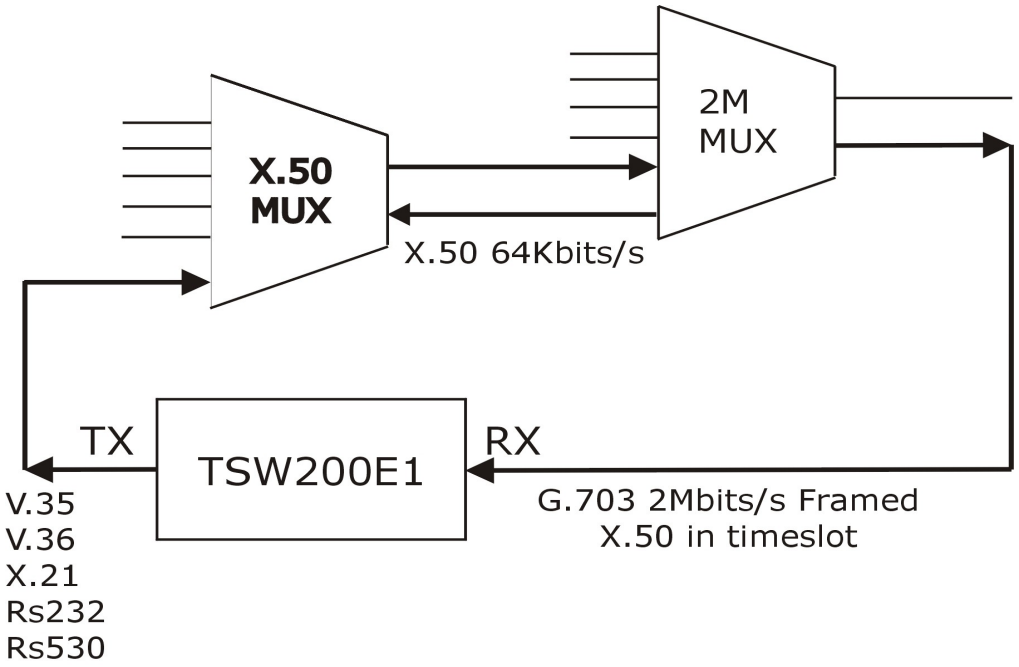
The test consists in sending a data pattern in the X.50 frame structure and checking if that same pattern is received at the chosen interface. The X.50 data stream transmission carrying the test pattern is done via the 64k G.703 interface. The test pattern is received from the demultiplexer, via the V.35/V.11, V.36/V.11, X.21/V.11 or RS530 interfaces.

Configuring the DEMUX test is very similar to configuring the TX/RX test. But only the receive interface and the transmission-related parameters can be changed. The clock source is always internal, for in this case the TSW200E1 must provide the clock.

The test results are presented in the same way as for the TX/RX test. Please check Section 2.2 for more details.

2.6 - Configuring and running the X.50 MUX Test at 2Mbps

The figure below exemplifies running the X.50 MUX test at 2Mbps:



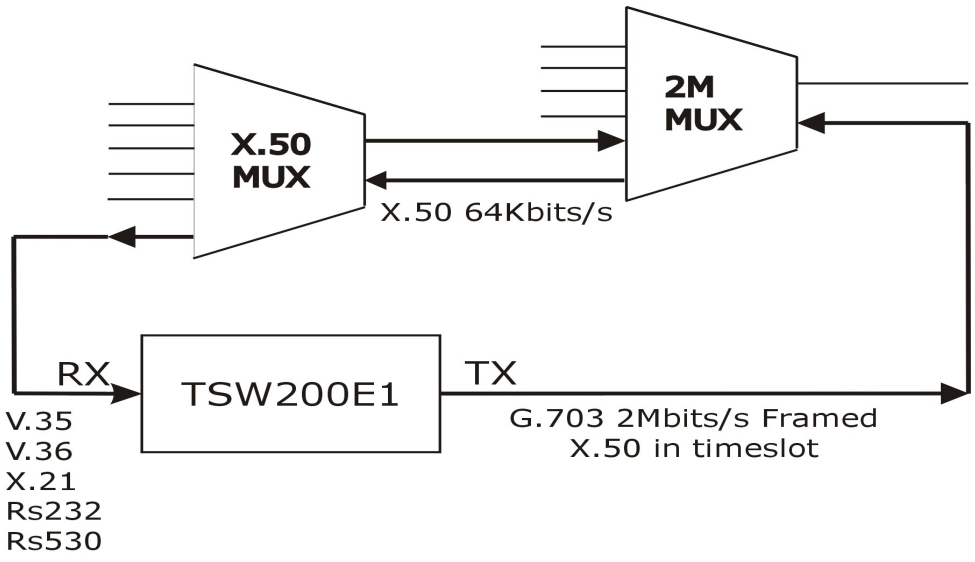
The test consists in sending a data pattern to the X.50 multiplexer and checking this same data pattern within the X.50 structure inserted in a PCM slot. In that way, the data pattern is sent via the interface chosen at the configuration screen and the reception is done by the G.703 2M interface.

Configuring the MUX test is very similar to configuring the TX/RX test. But only the transmit interface and the reception-related parameters can be changed. The clock source is always external, for it must be provided by the MUX and not by the TSW200E1.

The test results are presented in the same way as for the TX/RX test. Please check section 2.2 for more details.

2.7 - Configuring and running the X.50 DEMUX Test at 2Mbps

The following figure exemplifies running the X.50 DEMUX test at 2Mbps.



The test consists in sending a data pattern within the X.50 structure inserted in a PCM slot for the X.50 demultiplexer and checking this same demultiplexed data pattern. In this way, the data pattern is sent through the G.703 2M interface and data are received by the interface chosen at the configuration screen.

Configuring the DEMUX test is very similar to configuring the TX/RX test. But only the receive interface and the transmission-related parameters can be changed. The clock source is always internal, for it must be provided by the TSW200E1.

The test results are presented in the same way as for the TX/RX test. Please check section 2.2 for more details.

3 - Technical Terms Glossary

The meaning of many technical terms as used in this manual is now presented.

FAS (*Frame Alignment Signal)*

Used for timeslot 0 in alternated frames (even frames) for the 2 Mbps frames or in bit 7 of each X.50 frame octet.

ITU-T (International Telecommunication Union)

Sets rules and standards for telecommunication transmissions. CCITT successor.

Octet

Basic element of the X.50 frame. It is composed of 8 bits (one frame bit, six data bits and one status bit).

Protocol

Set of rules that determine the message format and the timing involved in the communication between two (or more) systems.

REMOTE ALARM

Remote alarm counter.

Appendix A: 64kbps X.50 Frame Structure

The X.50 frames of the divisions 2 and 3, according to the ITU-T X.50 Recommendation, are divided in octets defined in the following way:

B I T	7	6	5	4	3	2	1	0
	F	D	D	D	D	D	D	S

where:

F = Frame bit (see FAS word below)
D = Data bits
S = Status bit

For division 2, the frame is composed of 80 octets in the above format. For division 3 there are 20 octets only.

A.1. Division 2

For division 2 the frame sync word (FAS) has 80 bits distributed in bit 7 of each frame octet. The word is the following:

A	1	0	0	0	1	1	1	1	1	B	1	0	0	0	0	1	1	1	0
C	1	1	1	0	0	1	0	1	1	D	0	1	0	0	1	0	0	0	0
E	0	1	0	0	0	1	0	0	1	F	0	0	0	1	0	1	1	1	0
G	0	1	1	0	1	1	0	0	0	H	0	1	1	0	0	1	1	0	1

where:

A = Maintenance bit (= 1 indicates absence of alarm, = 0 indicates alarm)

B a H = Bits of unspecified use. For the TSW200E1, these bits have the following format:

B	C	D	E	F	G	H
1	1	0	0	1	1	0

The division 2 X.50 frame presents the following structure:

	Phases				
	1	2	3	4	5
Octets	0	1	2	3	4
	5	6	7	8	9
	10	11	12	13	14
	15	16	17	18	19
	20	21	22	23	24
	25	26	27	28	29
	30	31	32	33	34
	35	36	37	38	39
	40	41	42	43	44
	45	46	47	48	49
	50	51	52	53	54
	55	56	57	58	59
	60	61	62	63	64
	65	66	67	68	69
	70	71	72	73	74
	75	76	77	78	79

Each octet is transmitted at 64K/80 = 800 bps. As there are only six data bits, the data bit rate is 800 * 6 / 8 = 600 bps per octet. So, to transmit at 4800 bps, eight octets will be necessary.

The X.50 division 2 defines five different rates:

Octet Rate	Data Rate	Number of Octets
25600 bps	19200 bps	32
12800 bps	9600 bps	16
6400 bps	4800 bps	8
3200 bps	2400 bps	4
1600 bps	1200 bps	2

See in the following frames the possible options for the TX and RX Channel for each of the division 2 speeds. These frames display the combination of octets and phases that can transmit data for certain desired data rates.

For the 1200 bps rate:

	Phase				
Octet	**1**	**2**	**3**	**4**	**5**
1	0,40	1,41	2,42	3,43	4,44
2	5,45	6,46	7,47	8,48	9,49
3	10,50	11,51	12,52	13,53	14,54
4	15,55	16,56	17,57	18,58	19,59
5	20,60	21,61	22,62	23,63	24,64
6	25,65	26,66	27,67	28,68	29,69
7	30,70	31,71	32,72	33,73	34,74
8	35,75	36,76	37,77	38,78	39,79

For the 2400 bps speed:

	Phase				
Octet	**1**	**2**	**3**	**4**	**5**
1	0,20,40,60	1,21,41,61	2,22,42,62	3,23,43,63	4,24,44,64
2	5,25,45,65	6,26,46,66	7,27,47,67	8,28,48,68	9,29,49,69
3	10,30,50,70	11,31,51,71	12,32,52,72	13,33,53,73	14,34,54,74
4	15,35,55,75	16,36,56,76	17,37,57,77	18,38,58,78	19,39,59,79

For the 9600 bps data rate:

	Phase				
Octets	**1**	**2**	**3**	**4**	**5**
1	0,5,10,15,20, 25,30,35,40, 45,50,55,60, 65, 70,75	1,6,11,16,21, 26,31,36,41, 46,51, 56,61, 66,71,76	2,7,12,17,22, 27,32,37,42, 47,52,57,62, 67,72,77	3,8,13,18,23, 28,33,38,43, 48,53,58,63, 68,73,78	4,9,14,19,24, 29,34,39,44, 49,54,59,64, 69,74,79

To generate the 19200 bps rate, 32 octets are used. That means two phases must be allocated. So, the display will always show two phases.

A.2. Division 3

For division 3 the FAS word has 20 bits distributed in bit 7 for each frame octet. So, the word has the following format:

A 1 1 0 1 0 0 1 0 0 0 0 1 0 1 0 1 1 1 0

where:

A = Maintenance bit (= 1 indicates absence of alarm, = 0 indicates alarm)

The X.50 division 3 frame presents the following structure:

	Phases				
	1	**2**	**3**	**4**	**5**
Octets	0	1	2	3	4
	5	6	7	8	9
	10	11	12	13	14
	15	16	17	18	19

Each octet is transmitted at 64K/20 = 3200 bps. As there are only six data bits, the data bit rate is 3200 * 6 / 8 = 2400 bps per octet; so, to transmit at 4800 bps, 2 octets will be needed.

The X.50 division 3 defines four different rates:

Octet Rate	Data Rate	Number of Octets
25600 bps	19200 bps	8
12800 bps	9600 bps	4
6400 bps	4800 bps	2
3200 bps	2400 bps	1

See in the following frames the possible options for TX and RX Channel for each division 3 available rates.

For the 2400 bps data rate, the possible combinations are:

	Phase				
Octet	**1**	**2**	**3**	**4**	**5**
1	0	1	2	3	4
2	5	6	7	8	9
3	10	11	12	13	14
4	15	16	17	18	19

For the 4800 bps rate:

	Phase				
Octet	**1**	**2**	**3**	**4**	**5**
1	0,10	1,11	2,12	3,13	4,14
2	5,15	6,16	7,17	8,18	9,19

For the 9600 bps rate:

	Phase				
Octet	1	2	3	4	5
1	0,5,10,15	1,6,11,16	2,7,12,17	3,8,13,18	4,9,14,19

To generate the 19200 bps rate, 32 octets are used. That means two phases must be allocated. So, the display will always show two phases.